A Minimalistic CPU with DEEDS

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Memory mapping :

The bit 7 (MSB) of 8 bits addresses selects ROM or RAM :

- ROM = [00-7F] for the programs
- RAM = [80-FF] for the data

Instruction set :

	7654 3210		
00	0000 0000	LDA [address]	ACC = MEM [address]
01	0000 0001	ADD [address]	ACC = ACC + MEM [address]
02	0000 0010	CMP [address]	Compare ACC with MEM [address]
03	0000 0011		
04	0000 0100		
05	0000 0101	SUB [address]	ACC = ACC – MEM [address]
06	0000 0110		
07	0000 0111		
08	0000 1000	LDA constant	ACC = constant
09	0000 1001	ADD constant	ACC = ACC + constant
0A	0000 1010	CMP constant	Compare ACC with constant
0B	0000 1011		
0C	0000 1100		
0D	0000 1101	SUB constant	ACC = ACC – constant
0E	0000 1110		
0F	0000 1111		
13	0001 0011	STO [address]	MEM [address] = ACC
23	0010 0011	BRA address	PC = address
43	0100 0011	BRZ address	PC = address if zero
83	1000 0011	BRE address	PC = address if equal

Operations sequence :

0	1 0 0 0 0 0 0	Load Opcode Register : OPCODE = D7-D0
1	0 1 0 0 0 1 0	Increment Program Counter : PC = PC + 1
2	0 0 1 0 0 0 0	Load Operand Register : OPERAND = D7-D0
4	0 0 0 1 1 1 0	Push Address : A7-A0 = OPERAND
5	0 0 0 0 1 0 0	Load Accumulator : ACCU = operation result
6	0 0 0 0 0 1 0	Write Enable if (CODE == 00) : D7-D0 = ACCU
3	0 0 0 0 0 0 1	Goto if (CODE == 23 | 43 | 83) : PC = OPERAND

Tests programs :

- For ACC = 0 to 5 (test1.drs) :

```
LDA 00      00 08 00
ADD 01      02 09 01
CMP 05      04 0A 05
BRE 0A      06 83 0A
BRA 02      08 23 02
BRA 0A      0A 23 0A
```

- For ACC = 5 to 0 (test2.drs) :

```
LDA 05      00 08 05
SUB 01      02 0D 01
BRZ 08      04 43 08
BRA 02      06 23 02
BRA 08      08 23 08
```

- Memory read and write (test3.drs) :

```
LDA AA      00 08 AA
STO [80]    02 13 80
LDA BB      04 08 BB
STO [81]    06 13 81
LDA [80]    08 00 80
LDA [81]    0A 00 81
BRA 0C      0C 23 0C
```

- Arithmetic with memory (test4.drs) :

```
LDA 02      00 08 02
STO [80]    02 13 80
LDA 00      04 08 00
ADD [80]    06 01 80
SUB [80]    08 05 80
BRA 06      0A 23 06
```

- Comparison with memory (test5.drs) :

```
LDA 05      00 08 05
STO [80]    02 13 80
LDA 00      04 08 00
ADD 01      06 09 01
CMP [80]    08 02 80
BRE 0E      0A 83 0E
BRA 06      0C 23 06
BRA 0E      0E 23 0E
```