Digital Design Laboratory

A Musical Box on FPGA designed with Deeds

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**DITEN – University of Genoa, Italy, **Metropolia University of Applied Sciences, Finland*

The software tools presented are available
free of charge to all interested parties at:

http://www.esng.dibe.unige.it/deeds/

Introduction

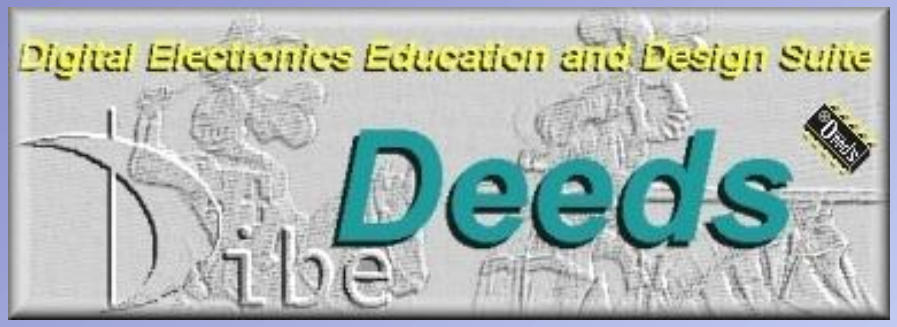
- The introduction of ***Field Programmable Gate Arrays*** (FPGA) in a first year course of digital design in ICT engineering is nowadays advisable.
- It is not easy to build good foundations on logic design just by completely migrating the traditional schematic, simulation and bread-board based prototyping to VHDL based FPGA design flow.
- **Deeds** *(**Digital Electronics Education and Design Suite**)* makes the process of FPGA configuration straightforward and compatible with the beginners' skills.
- Tutorials guide students in the process and, at the same time, provide a synthetic introduction to FPGA projects.

FPGA and beginners' skills

- Our approach fills an important learning gap in early exposure to FPGA, by skipping the pre-requisite of a hardware description language or the proficiency in high-level programming languages.
- **Deeds** integrates FPGA configuration and testing into its interactive design and simulation flow, making combinational and sequential design, as well as microprocessor core programming, demonstrable through physical FPGA boards.
- The process achieves appreciable effects and it is fully compatible with the beginner's skills.

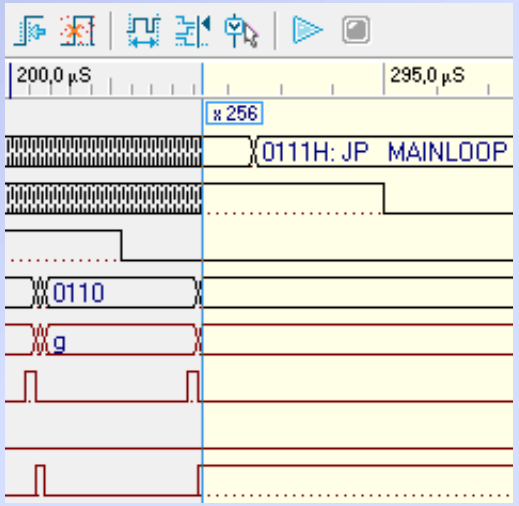
Tutorials and projects

- Tutorials and projects, designed for flexibility and ease of self-learning, open up many possibilities to hands-on experiments.
- Students experience digital system designs of different complexities, involving combinational logic, FSM and microprocessor programming.
- Freshman level students can easily understand the low-level behavior of embedded systems, a good foundation for successive courses on design languages, IP cores, hardware-software co-design.



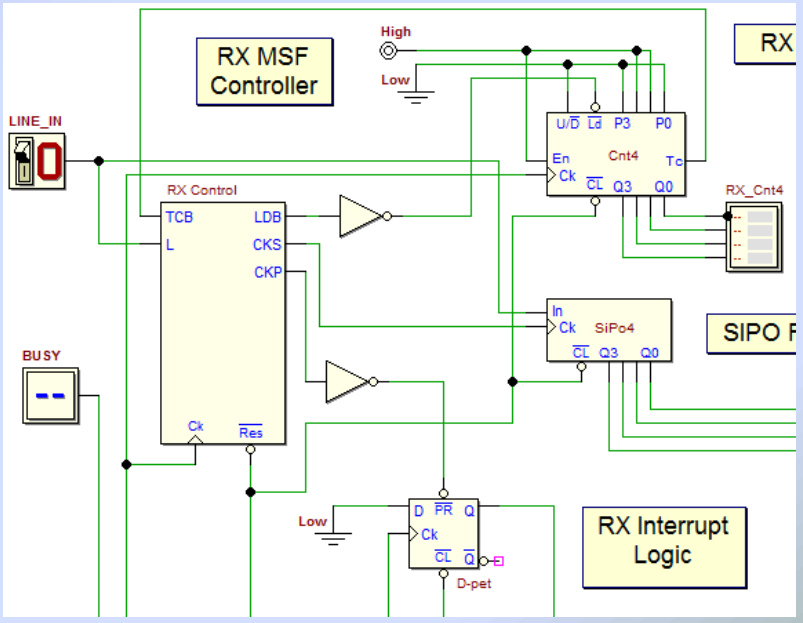
- ***Deeds*** is developed at DITEN (ex DIBE), University of Genoa
- The suite is composed by three simulators and a wide collection of associated ***learning material*** to learn-by-doing and practice with:
  - ***Combinational and sequential logic networks***
  - ***Finite state machine design***
  - ***Embedded microcomputer interfacing and programming***
  - ***FPGA programming (exporting projects to EDA tools)***

Deeds: the simulation tools



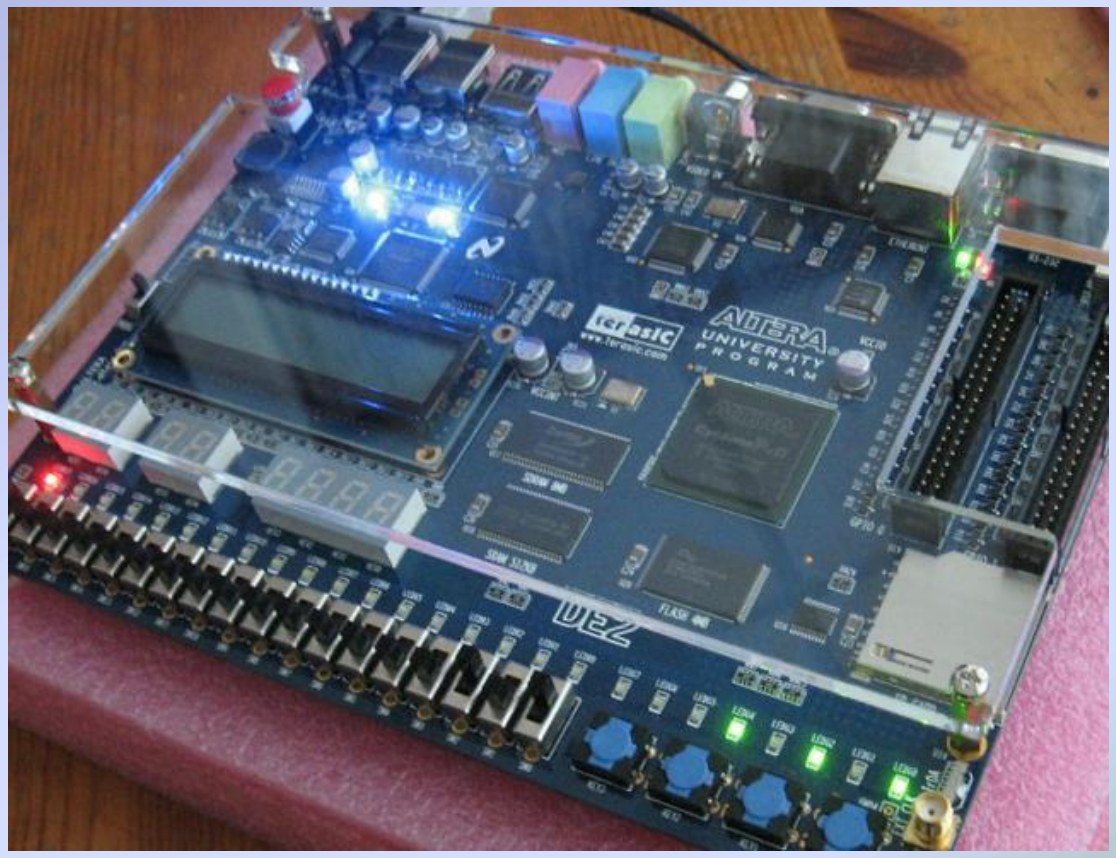
- d-DcS Digital Circuit Simulator
- d-FsM Finite State Machine Simulator
- d-McE Microcomputer Emulator

- The three simulators are *fully integrated*, to design and simulate *digital systems* with *standard logic*, *finite state machines* and *microcomputers.*



Deeds: FPGA prototyping

- **Deeds** allows testing of projects by implementing them in FPGA boards (Altera DE2 in the picture)
- The process does not require the user to be familiar with FPGA-specific development software.



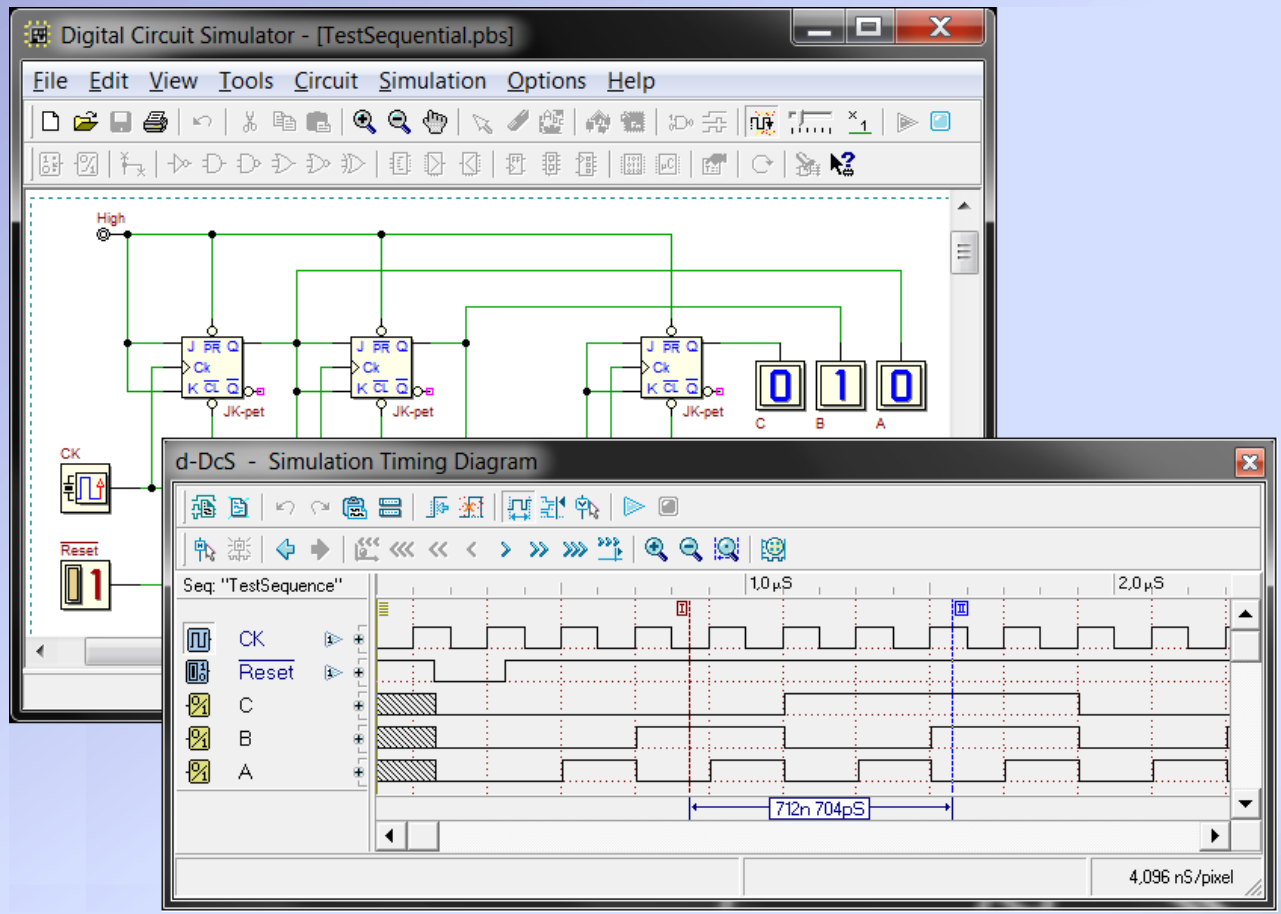
Deeds: FPGA tutorials and proiects

#	*Deeds* Introduction to Field Programmable Gate Arrays
1	***Tutorials:*** Circuit Prototyping on Altera DE2 Board New! Sequential Circuit Testing on Altera DE2 Board New! Microcomputer Testing on Altera DE2 Board New!
2	Analysis and implementation on FPGA of a 12-bits counter New!
3	A light controller on FPGA
4	Serial Transmitter and Receiver on FPGA
5	Asynchronous Serial Transmitter and Receiver, on FPGA New!
6	Push-button controlled byte generator on FPGA New!
7	Emulation of a Register/Counter on FPGA New!
8	Emulation of a Universal Shift Register on FPGA New!
9	Asynchronous Serial Transmitter and Receiver, interrupt based, on FPGA New!
10	Digital Waveform Generator, on FPGA New!
11	Asynchronous Serial Line Data Processor, on FPGA New!

Tutorials: Circuit Prototyping on FPGA (1)

A few tutorials provides instructions on how to transfer a Deeds project to the board.

After a preliminary simulation phase, useful to understand the behavior of the network under test, the student can prove its functionality on a real circuit…

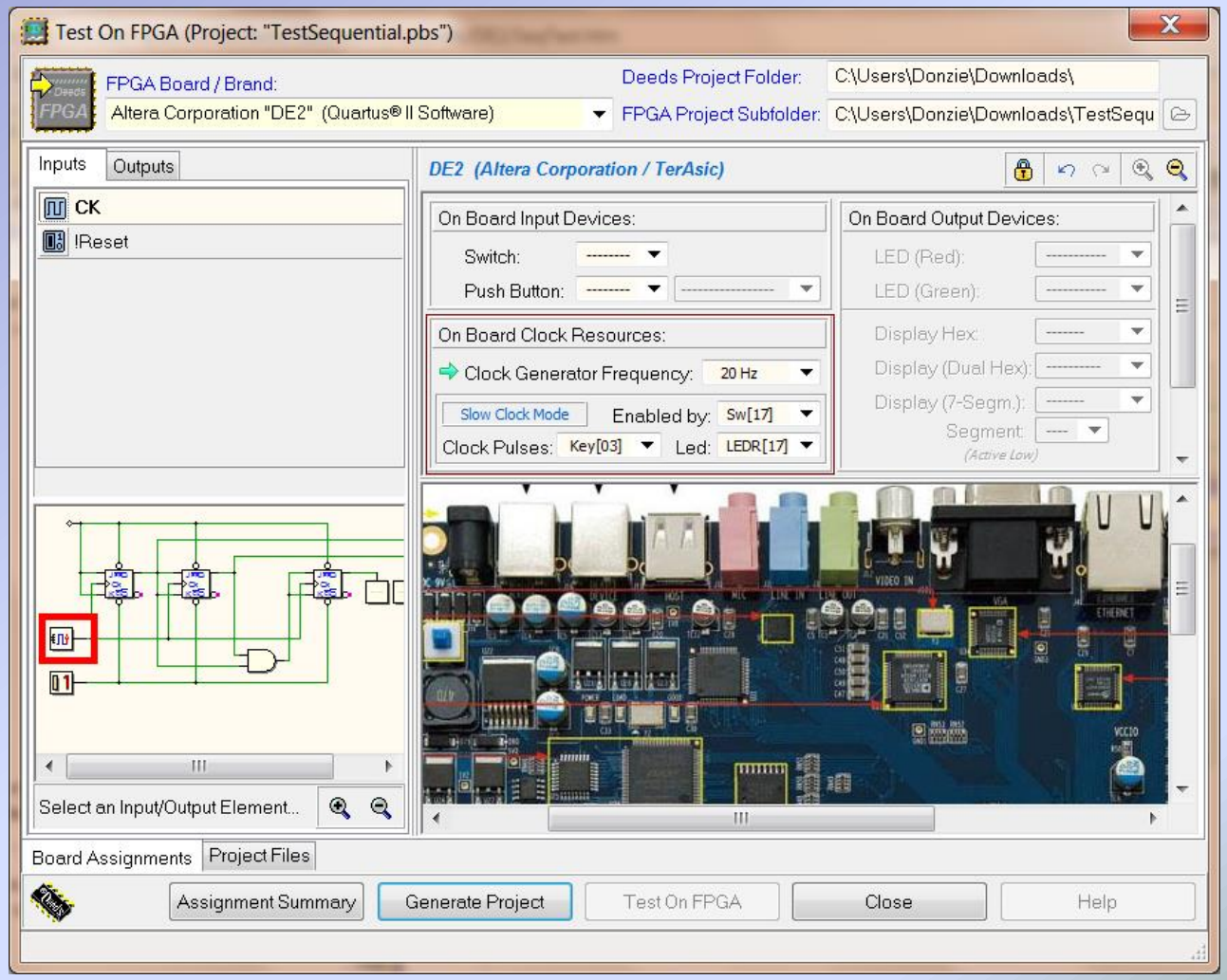


Tutorials: Circuit Prototyping on FPGA (2)

With the **Test on FPGA** dialog window the user can assign real board resources to the Deeds schematic.

In the tutorials, to simplify the process, this assignment is already done.

So, by clicking on **Generate Project**…

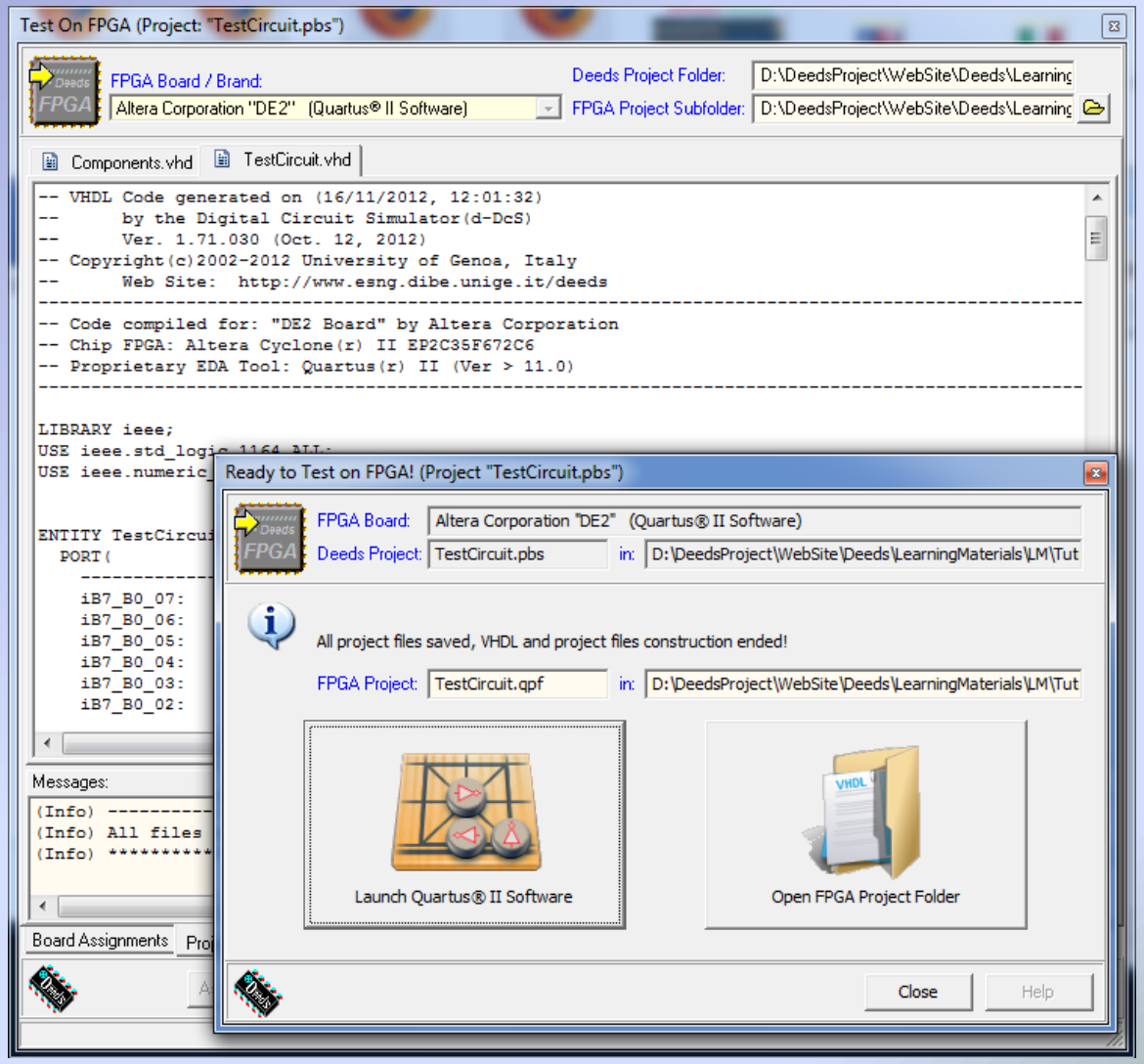


Tutorials: Circuit Prototyping on FPGA (3)

…by clicking on **Generate Project** the Deeds will create all the VHDL code and the project files necessary for the Altera Quartus® II software.

Students, at this time (if they wish so), can examine the VHDL code but...

…they can just launch Quartus® II from the dialog box.



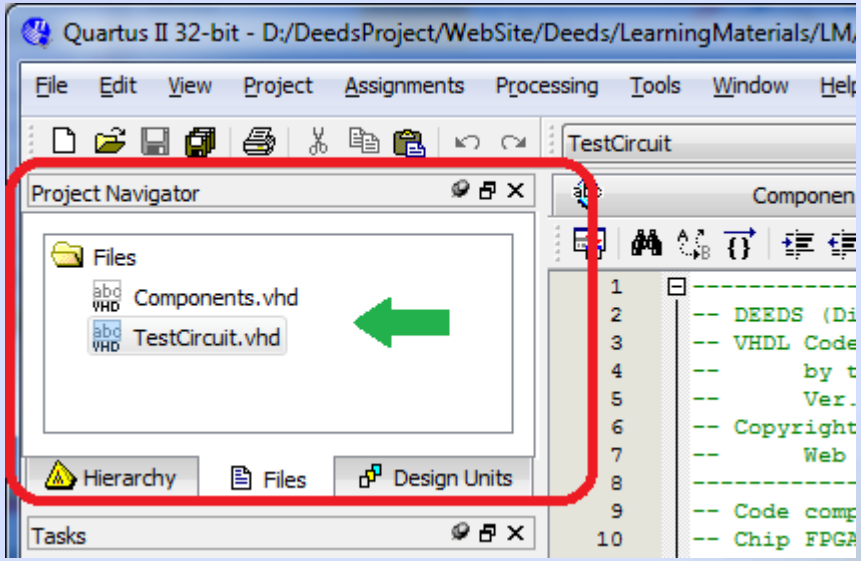
Tutorials: Circuit Prototyping on FPGA (4)

The project in Quartus® II is ready to be compiled.

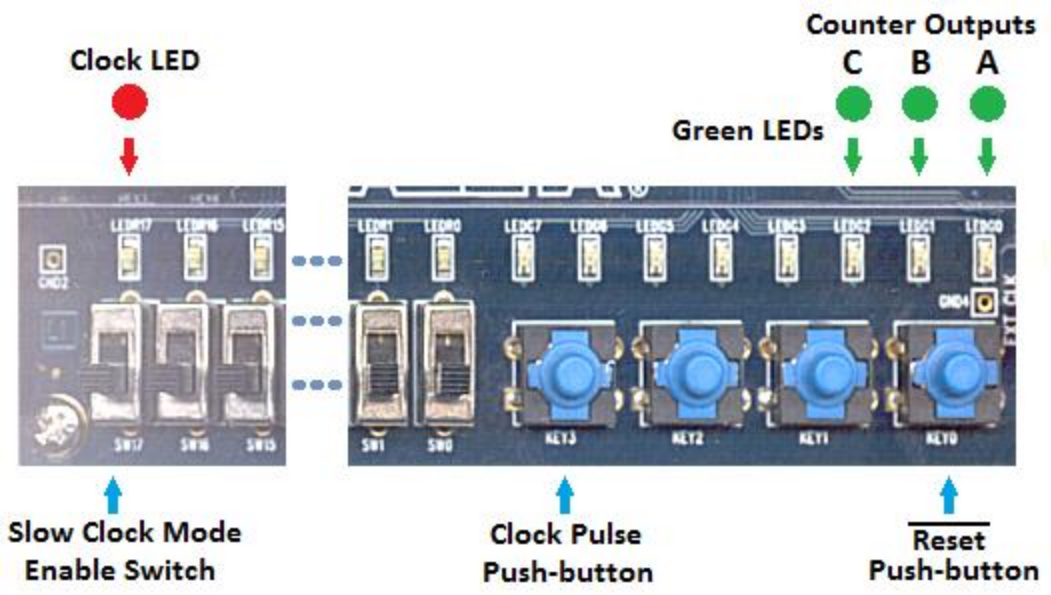
The **top VHDL file** contains the ***structural*** description of the digital network schematic.

The other **VHDL** files collect the ***behavioral*** descriptions of all the components used by the network, included Finite State Machines, Micro-Computers, ROM contents, etc.

After the compilation of the project, Quartus® II allows to transfer the circuit to the DE2 **FPGA board**.



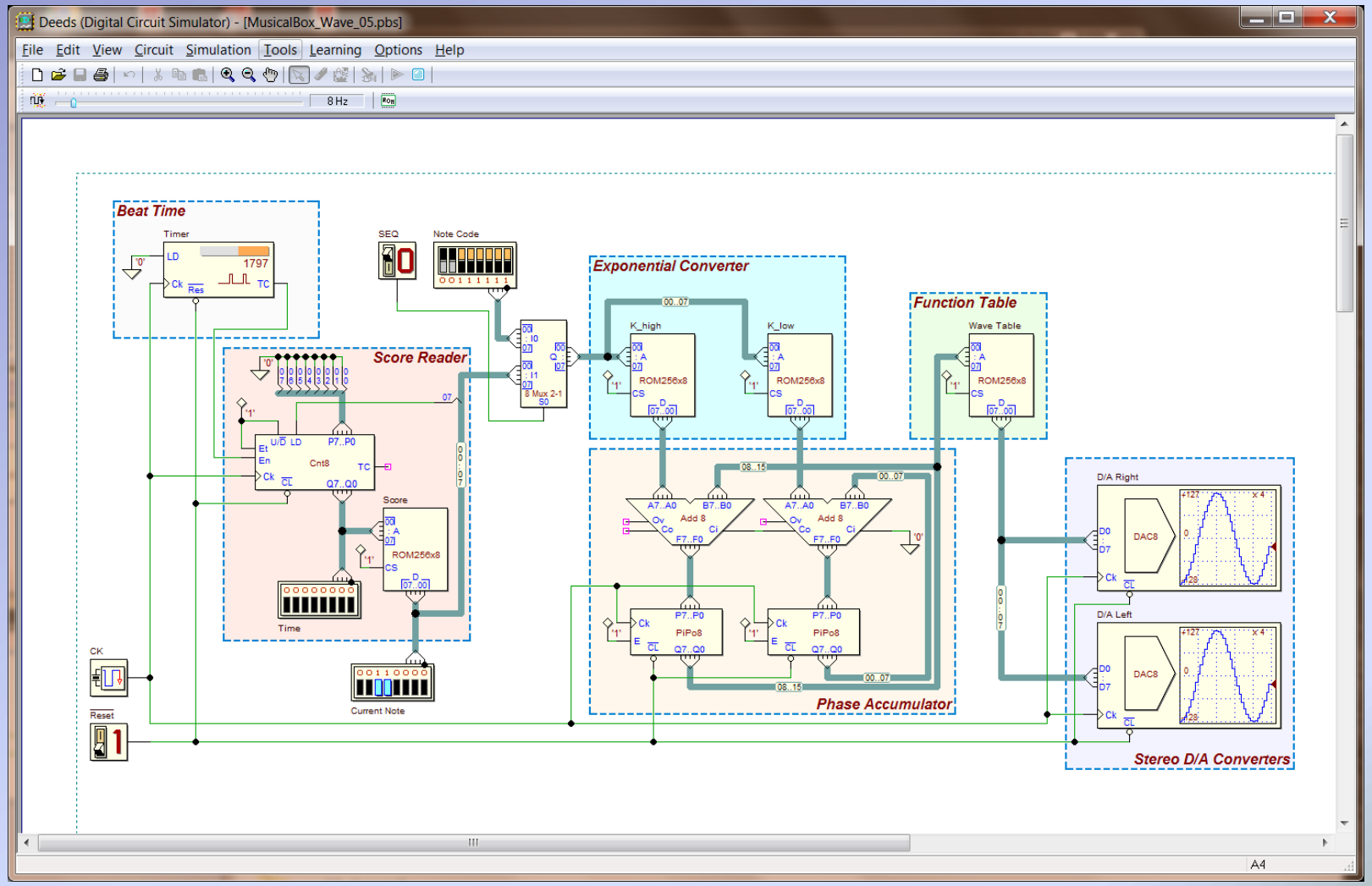
Tutorials: Circuit Prototyping on FPGA (5)



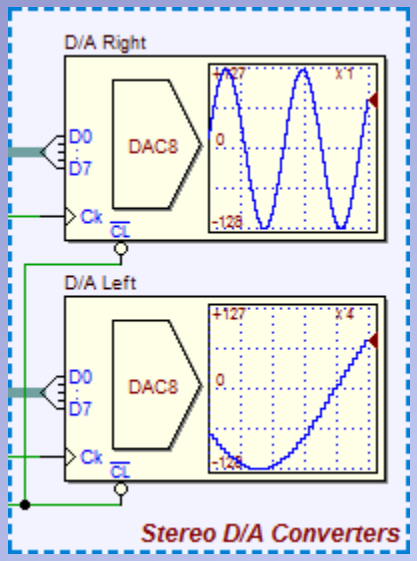
Lab assignments always include a board view of the I/O of the circuit under test.

Switches, pushbuttons and LEDs of the FPGA board are suggested to be used as a “control panel” for the testing the network.

A Digital Design Laboratory Session:
A Musical Box on FPGA



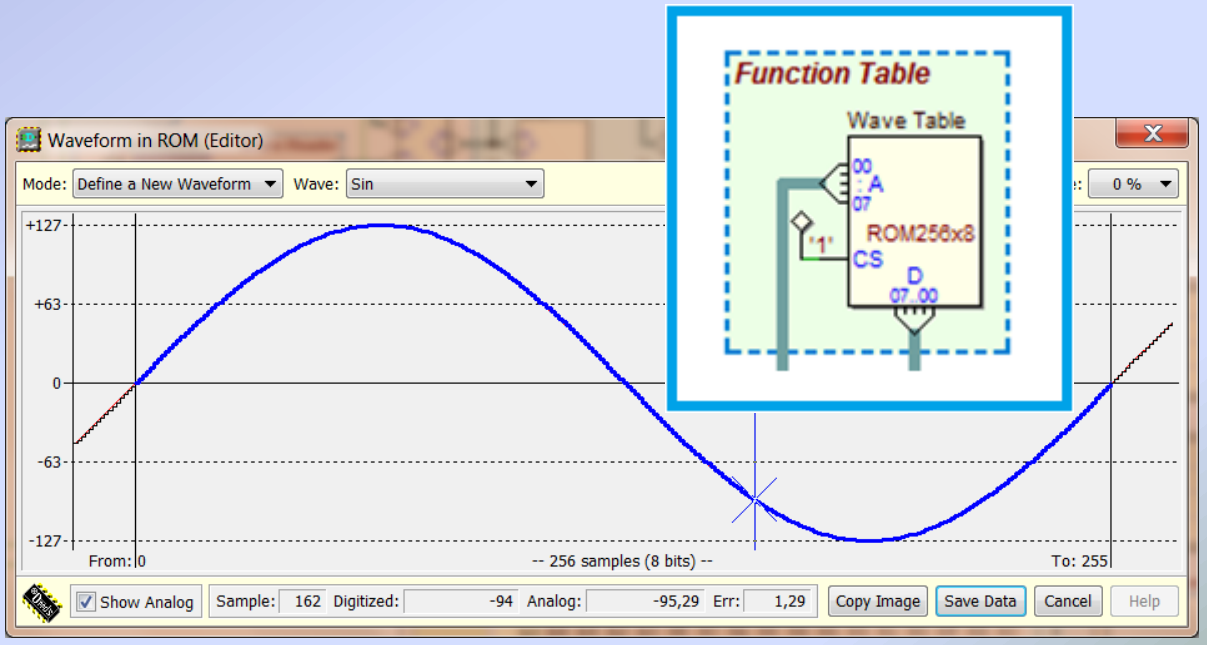
The Sine Waveform generator



Two outputs Digital to Analog Converter (DAC):

- 8 bit DACs
- Sampling clock frequency = 20 KHz
- Animated Output Waveforms

In the figure the Function Table, stored in a 256x8 ROM memory, contains the samples of a cycle of sine wave.



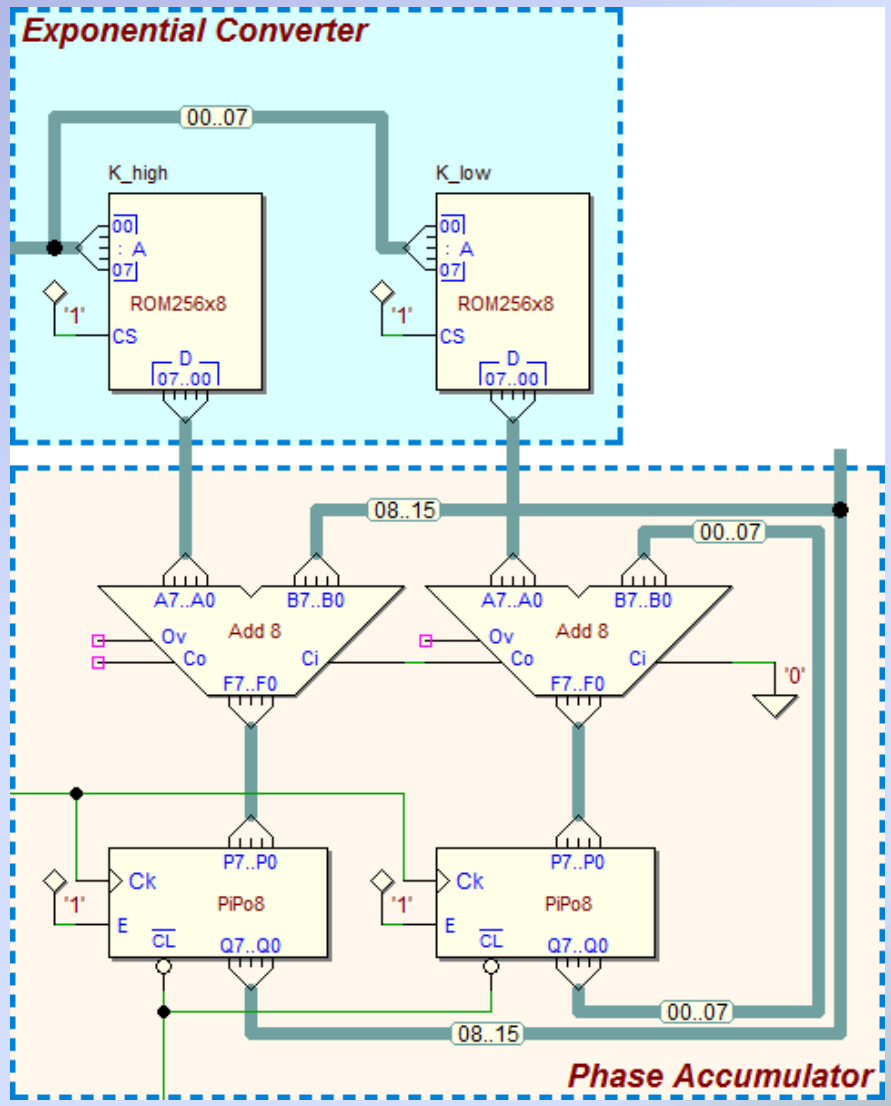
The Waveform Frequency Control

Addresses for the Function Table ROM are generated by a recursive 16 bits adder: the **Phase Accumulator**.

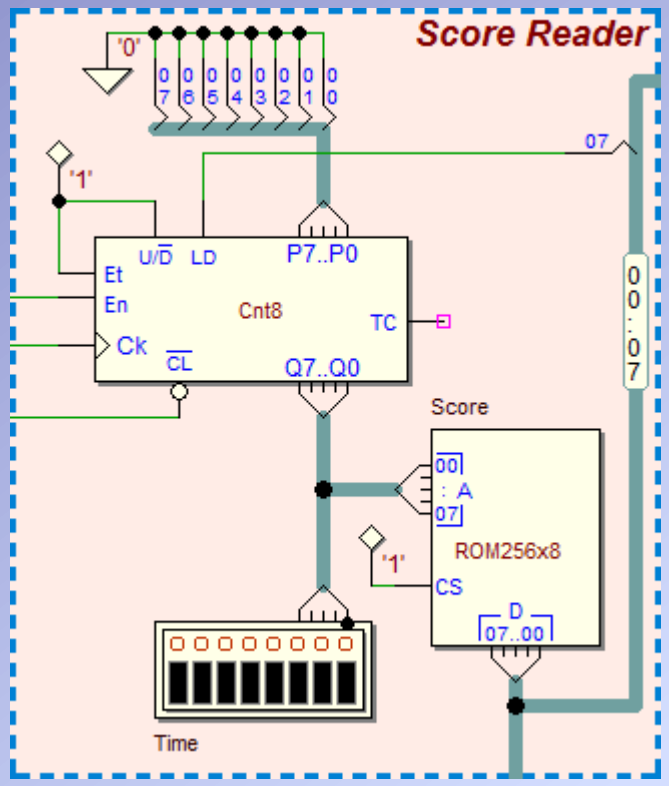
It calculates, at every clock, the current phase angle of the sine wave to be generated.

The Phase Accumulator receives a parameter proportional to the generated frequency.

Its value is given by an exponential conversion table (stored in two 256x8 ROMs), that receives the **Musical Note Code** as table index.



The Melody Generator

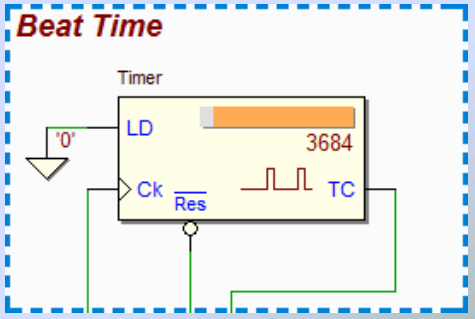


The **Musical Note Codes** are generated by a ROM, addressed cyclically by a counter.

The 256x8 ROM contains the musical melody to be played, as sequence of **standard MIDI note codes**.

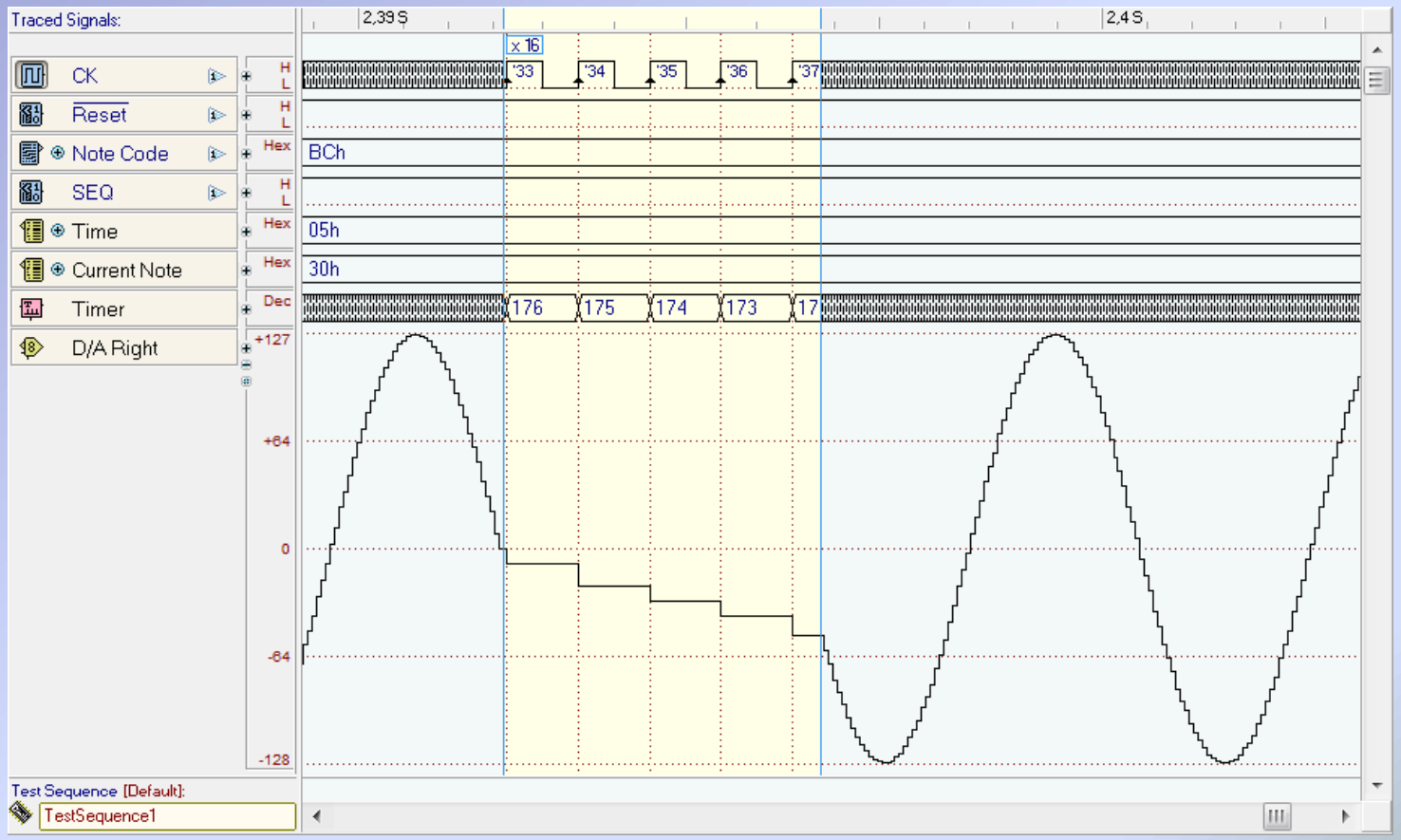
The melody is restarted from the beginning when a refrain code is read from the ROM.

The **Beat Time** of the note sequence is given by another counter, in fact, the **Metronome** of the generator.

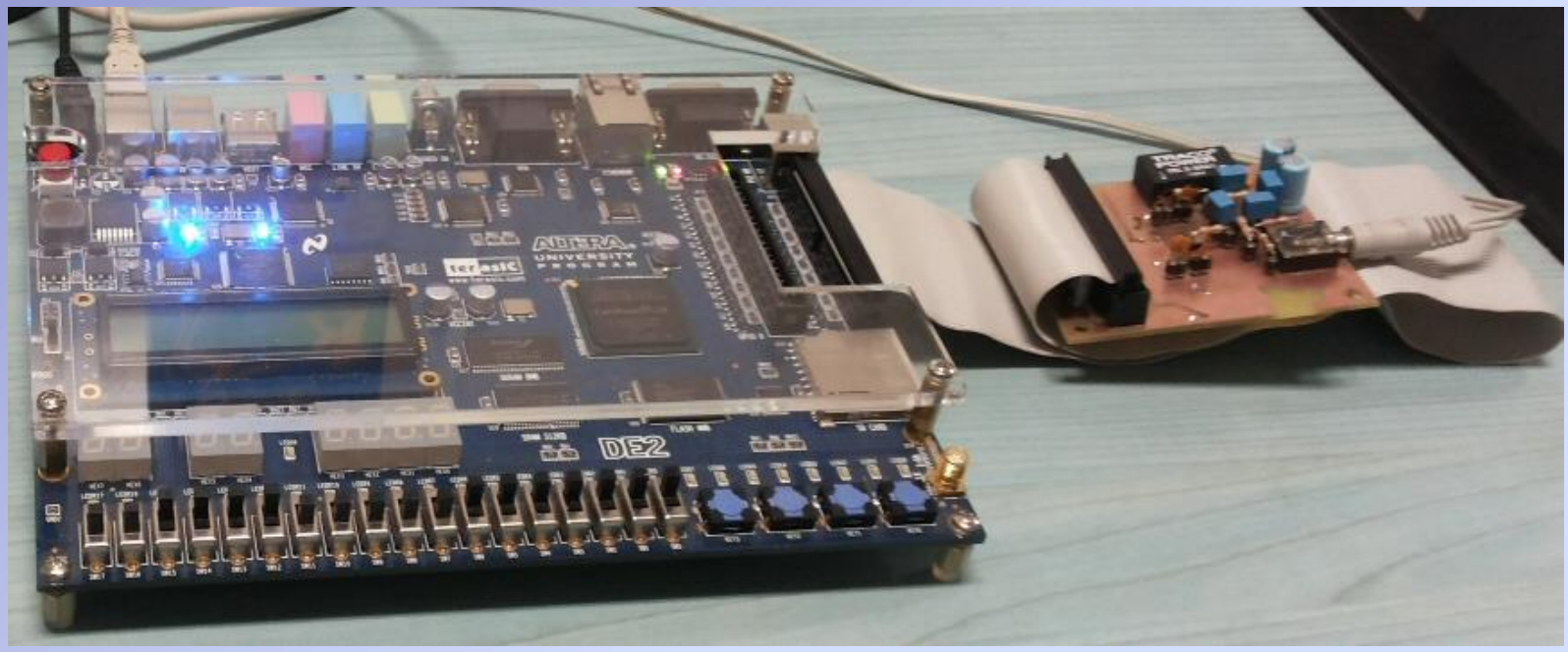


Timing simulation of the generator

The output of the Musical Box can be observed on the ***Deeds*** simulator **Timing Diagram**, almost as it were an analog signal.



The Musical Box prototype



The **Musical Box** prototyped on an Altera DE2 board (on the left side), connected to the stereo DAC module (on the right).

Tentative assessment of results

- In our teaching activity the introduction of novel or updated technical and pedagogical material is almost continuous. Therefore, comparisons with former educational situations or, worse, quantitative evaluations of the results are not possible.
- We can summarize here the observations resulting from our deep interaction with students activities.
- Deeds FPGA extension works properly. Students have no problems with the compilation of the files and the operation of the DE2 boards.
- The tutorial material guiding the experiments proved to be exhaustive and easy to understand.
- Students show a very strong interest for the laboratory sessions using the FPGA.

Deeds FPGA experience: conclusions

- Deeds has the possibility to export and test project on FPGA boards without the need of familiarity with FPGA and its development tools.
- Our approach is a solid introduction to understanding the low-level behavior of embedded system, bridging the gap with the design of more complex systems, using high level languages, IP modules, hardware-software co-design.
- The VHDL code generated by Deeds facilitates the transition from schematic entry to hardware description languages.

Impact of Deeds (1)

- Deeds is the work mainly of one dedicated person (Giuliano Donzellini) who wrote its more than 200,000 lines of code and maintains and expands it continuously.
- Deeds has been made available free of charge to institutions and person and it has been adopted by universities and secondary technical education schools.
- Tutorials and projects are available in Italian and English.
- Deeds educational materials have been translated and published in Turkish (Çizgi Elektronik,Istanbul), Spanish, Catalan and Italian.

Impact of Deeds (2)

The Deeds has been and it is used now in several European universities:

- Metropolia University of Applied Sciences (Helsinki, Finland)
- University of Deusto (Bilbao, Spain)
- School of Business and Engineering Vaud (Switzerland)
- Inholland University of Applied Sciences (Netherlands)
- Universidad de Las Palmas de Gran Canaria
- University of York (U.K)
- University of Sofia, Bulgaria
- Technological Education Institute of Piraeus, Athens

Impact of Deeds (3)

- Deeds has been used by thousands of students in Italy and abroad, from hands-on tutored laboratories to project-based learning and distance education.
- The addition of the PFGA prototyping has provided new life to its existing large depository of projects.
- The fact that teachers roles overlaps with developers roles guarantees the continuity between the tools and the educational situations.

How to get tools and materials (for free)

- All Deeds projects (in English and Italian) are available at:
  - http://www.esng.dibe.unige.it/deeds/LearningMaterials
- FPGA projects are indexed here:
  - http://www.esng.dibe.unige.it/deeds/FPGA

Send a mail to the authors:

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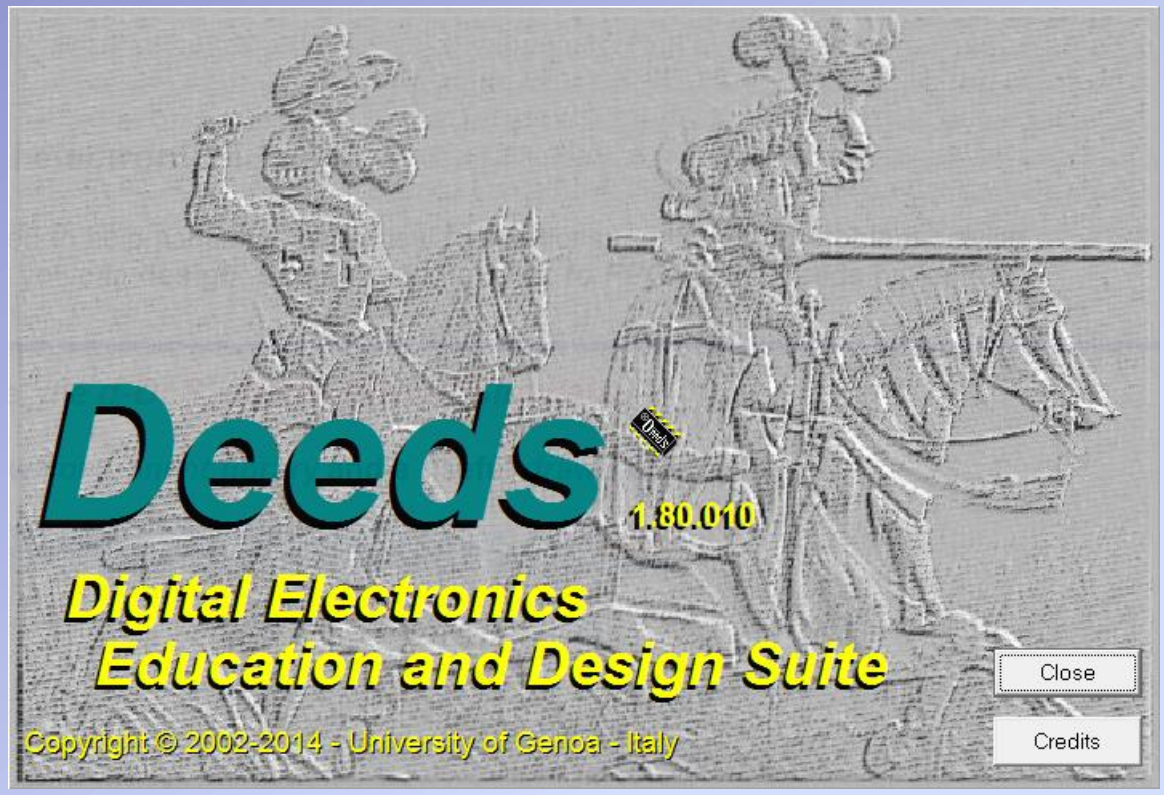
Thank you for your attention!



"The Deeds of Gallant Knights"
This image from a picture of G. David, XVI Century
Paris, Musèe de l'Armèe

We thank Altera Corporation for the generous donation of the DE2 development boards that have made possible an extensive experimentation in the lab.