

A Bottom-up Approach to Digital Design with FPGA

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http://www.esng.dibe.unige.it/deeds

Test On FPGA (VHDL top file: "CounterFF.pbs")

Testing

DE2 board

All files saved, VHDL conversion ended!

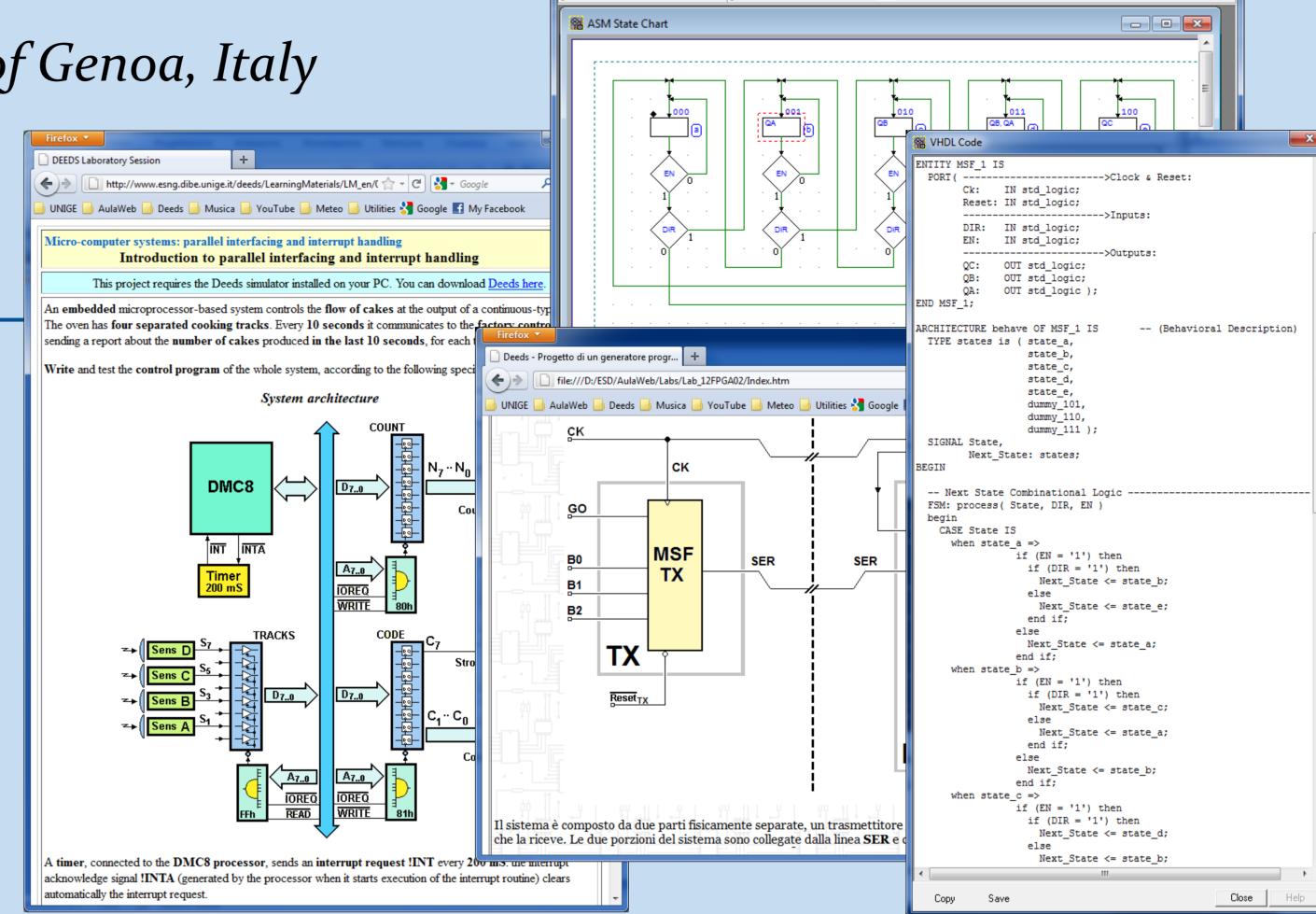
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D:\Donzie\Paper\A2011\IEEE_MSE\Deeds\CounterFF.VHDL

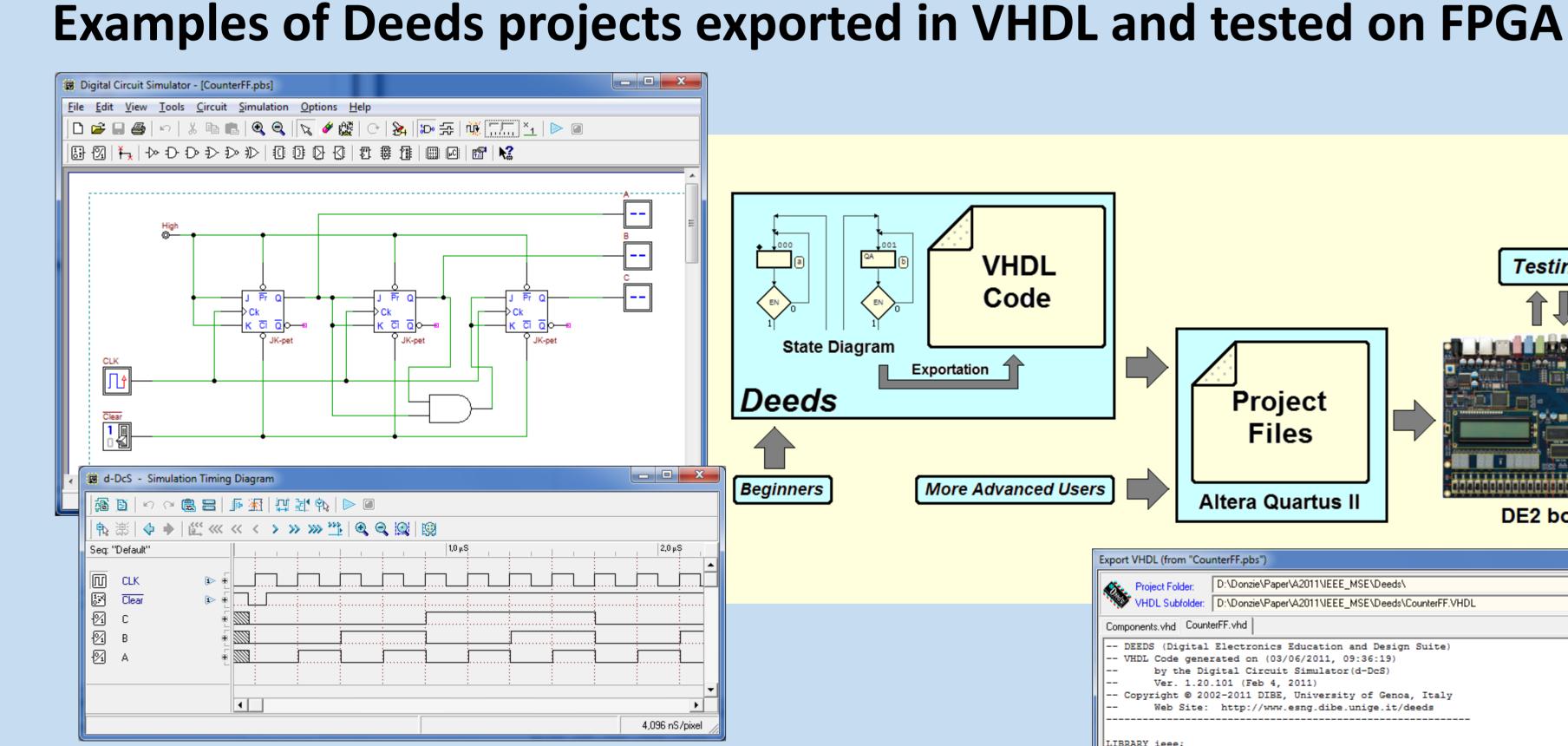


Deeds (Digital Electronics Education and Design Suite): VHDL generation and testing on FPGA

- Deeds is a learning environment based on three integrated simulators with good features and a simple user interface.
- ■Deeds is associated with a repository of learning material and application projects, available on the web.
- ■Deeds guides learners from simple gates circuits to the hardware/software foundations of embedded systems.
- •A new extension allows to export a project in VHDL format and to test in a FPGA board.
- •An Expert allows the choice of the FPGA board and its configuration for the circuit under test.
- Beginner learners can test Deeds projects without a previous knowledge of VHDL and FPGA proprietary software.
- •More advanced students still have the choice of interacting directly with the FPGA development system.



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A Deeds project ready to be tested on FPGA

References

G. Donzellini, D. Ponta: "From Gates to Embedded Systems: a Bottom-up Approach to Digital Design", "VIII 2009 International Conference on Microelectronic Systems Education – IEEE MSE09", San Francisco, California (U.S.A.), pp.61-64, 25-27 July 2009

G. Donzellini, D. Ponta, "A Virtual Laboratory for Digital Design", International Journal of Online Engineering (iJOE), Vol. 4, No. 2, ISSN 1861-2121, http://www.online-journals.org/i-joe, 2008

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The Deeds VHDL generator

USE ieee.std_logic_1164.ALL;

IN std_logic;

IN std_logic;

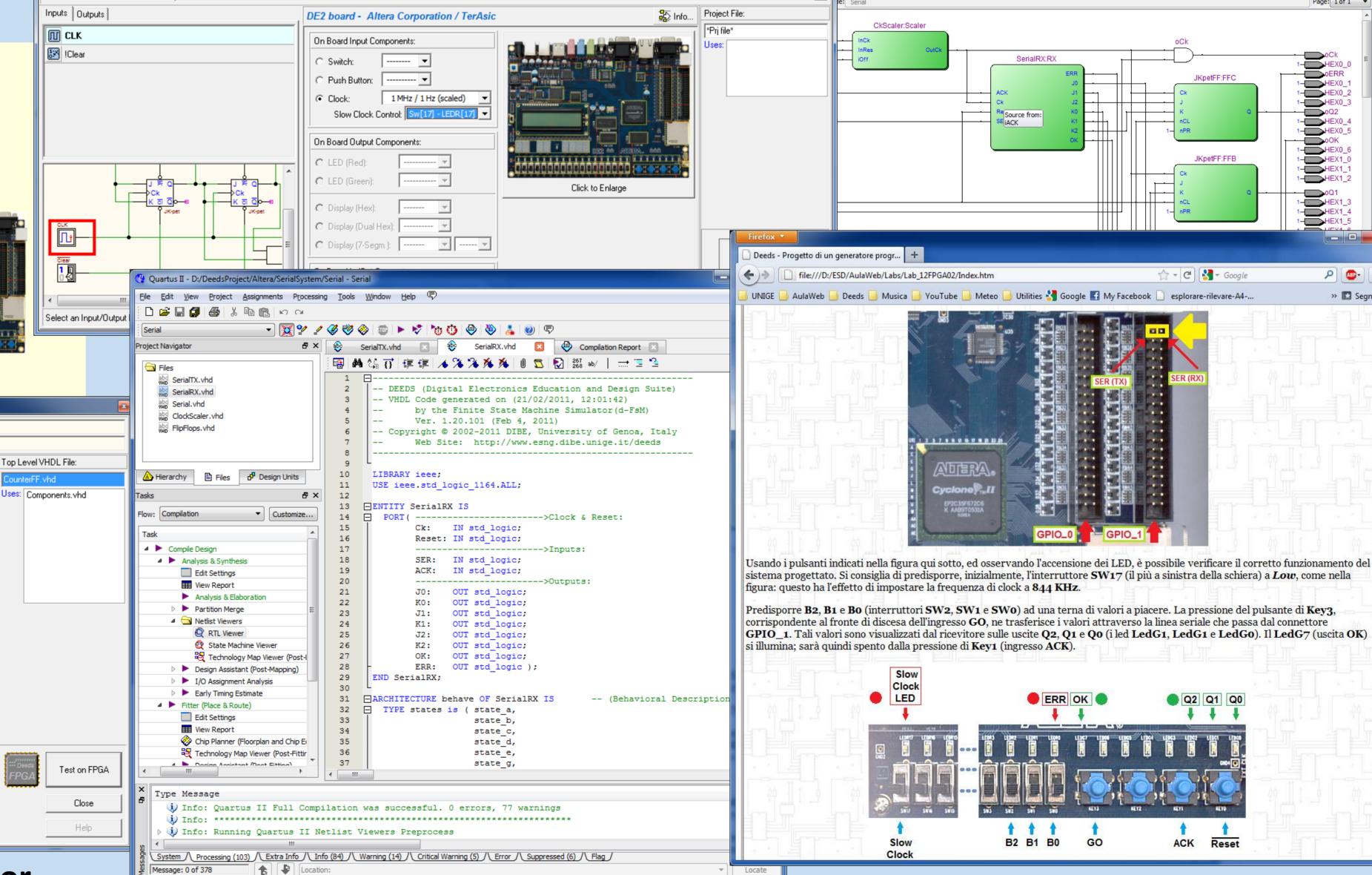
OUT std logic

OUT std_logic

Info) Top level structural VHDL description file loaded ("CounterFF.VHD")

ENTITY CounterFF IS

END CounterFF



RTL view of the project (top) and on board testing on the Terasic DE2 (bottom)

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The Deeds FPGA Expert (top) and the project opened in Altera Quartus II© (bottom)